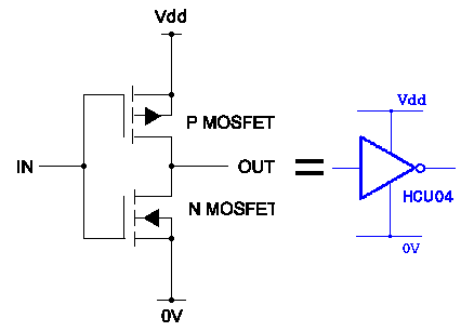# IC CRYSTAL OSCILLATOR CIRCUITS

The majority of IC's with built in crystal oscillator circuits use the Gated Pierce design where the oscillator is built around a single CMOS inverting gate. For oscillator applications this is usually a single inverting stage comprising one P channel and one N channel enhancement-mode MOSFET, more commonly known in the digital world as an Un-Buffered inverter (see Fig. 1). It is possible to use a Buffered inverter (usually comprising three P-N MOSFET pairs in series) but the associated gain of many thousands will lead to a potentially less stable finished oscillator.

Fig. 1

A practical oscillator circuit is shown in Fig. 2 comprising the Un-Buffered inverter, two capacitors, two resistors and the Quartz Crystal. To understand how this oscillator works the CMOS inverting gate must be considered as a linear amplifier with gain, phase and propagation delay constraints, not as a logic device working with 1's and 0's.
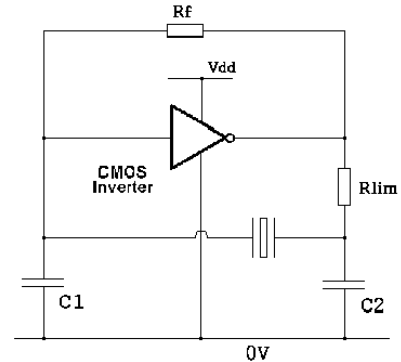
Fig. 2

Fig. 3 shows the DC Transfer Characteristics (Vin vs. Vout) and DC Bias Point line of an Un-Buffered HCMOS inverter 74HCU04. At 3.3V and a 1MΩ for Rf, the inverter will sit with its input and output voltages at ~1.65V. This inverter is now said to be biased in its linear region. A small change of the input voltage will be amplified by the gain and appear as a larger change in the output voltage.
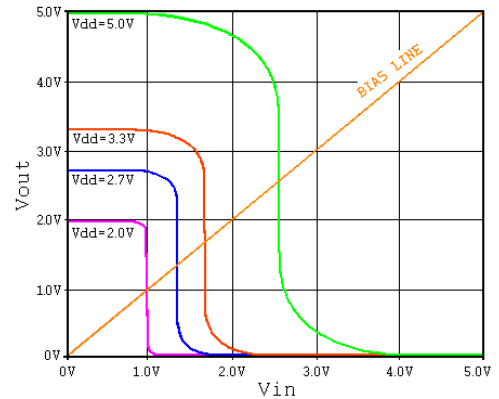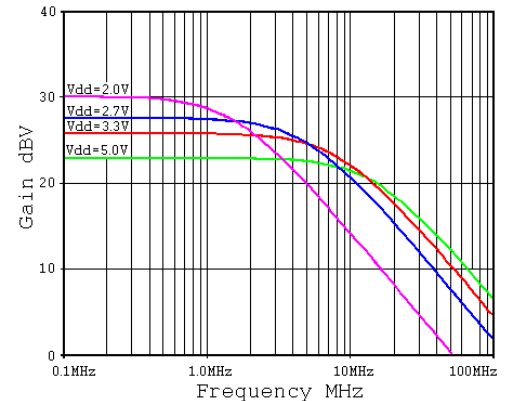
Fig. 3

Fig. 4 shows a typical set of Open Loop Gain curves for the same 74HCU04. At 3.3V the inverter has a gain of 20 (26 dBV) from DC to 2MHz, with a 3dB roll off frequency of 8.5MHz, and still appears to have gain beyond 100MHz.

Fig. 4

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For this biased inverting gate to be used as an oscillator it must have sufficient gain to overcome the losses of the feedback network (C1, C2, Rlim and Quartz Crystal in Fig. 2) , enough Negative Resistance at the frequency of oscillation to over come the crystals Equivalent Series Resistance, and the phase shift around the whole circuit must be 360°. It is tempting to think this 74HCU04 inverter could be used to make an oscillator that works beyond 100MHz as it has enough gain at 3.3V but in reality it would only be practical to make a stable oscillator up to ~20MHz due to the various phase shifts around the oscillator loop.

The analysis of this circuit is difficult to generalise as it is very dependant on the family of CMOS gate used and the internal construction of that particular CMOS family. All CMOS inverting gates have an input capacitance, an output capacitance, an output 'resistance', and a propagation delay, all of which effect the choice of C1, C2 and Rlim in Fig. 2 and ultimately the upper working frequency of the oscillator. The choice of biasing resistor Rf is usually between 1MΩ and 10MΩ, to low a value will effectively appear across the Crystal and may cause the Crystal to oscillate on a spurious or overtone frequency.

Consider a 20MHz crystal with an ESR of 15Ω, a C0 of 3pF and requiring a load capacitance of 20pF with a crystal power dissipation of approximately 100µW.

Starting with the desired load capacitance of 20pF this can be approximated as C1 + gate input capacitance (1 to 5pF being typical values) in series with C2. The ratio of C1 to C2 will affect the gain and crystal power dissipation. A good starting point is C1≈C2. To increase loop gain (and reduce crystal power dissipation) make C1 < C2. This generates sensible starting values of C1 = 33pF, C2 = 47pF for a load capacitance of 20pF with the gate having an input capacitance of ~3pF.

Using these capacitor values without Rlim will make a working oscillator but the crystal drive power will be about 1mW, over 10 times the 100µW recommended value for this design, and for modern AT strip crystals potentially catastrophic. Adding Rlim will reduce the crystal drive power but also reduce the loop gain and negative resistance to a limit where the oscillator will not start. There is no simple equation to predict the actual crystal power dissipation but as a rule of thumb, for selecting Rlim, start with Rlim = the reactance of C2 at the desired oscillator frequency (in this case C2 = 47pF = 170Ω at 20MHz). Fig. 5 is a plot of the actual crystal power dissipation for varying values of Rlim for the above design. At 500Ω for Rlim the oscillator is very close to not starting.

Fig. 5
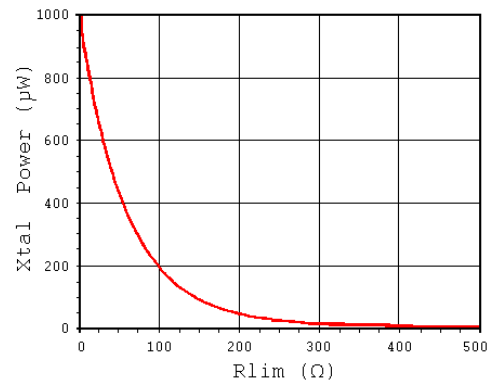
We have already shown the biased 74HCU04 inverter has sufficient gain up to 100MHz at 3.3V so we need to consider where the 360° of phase shift comes from to make our oscillator. The gate is already 180° by virtue of being an inverter but we must add to this figure the phase shift due to it's propagation delay and the additional phase shift due to the fact we are working beyond the gates flat gain vs. frequency portion of the curves in Fig. 4.

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The phase shift due to the propagation delay is calculated as:-

Phase Shift = Propagation Delay * Working Frequency * 360°

And the phase shift due to the working frequency is calculated as:-

Phase Shift = Tan^{-1}(F_{osc} / F_{3dB})

For this 20MHz design this equates to 35° for the propagation delay and 67° for the working frequency. The remaining 72° is generated by Rlim + the inverting gates output 'resistance' and the PI network comprising C1, C2 and the Quartz Crystal. It is the additional phase shift through the inverting gate that sets the upper working frequency limit for this design.

Checking the 'goodness' of the chosen design is also virtually impossible without specialised test equipment. One check for 'goodness' is to monitor the waveforms at the input and output of the inverting gate. This will require a high bandwidth oscilloscope and a specialised probe. The normal x10 oscilloscope probe will have an input impedance of ~10 MΩ in parallel with 10pF. The 10 MΩ will form a DC potential divider to GND with the 1 MΩ bias resistor Rf which will alter the oscillators bias point. The 10pF will appear directly across C1 when measuring the inverter input waveform making C1 = 43pF, not the designed 33pF. Any trace observed on the oscilloscope will be completely invalid (and most likely the probe will stop the oscillator from working anyway). A better choice of oscilloscope probe is an 'Active' or 'FET' probe which has a high input impedance buffer built into the probe tip. The input impedance of an 'Active' probe is typically >10 MΩ in parallel with <2pF, but as before the effect of using this probe must be taken into account when probing the oscillator. For this design the waveforms required (assuming a suitable probe is used that will not alter the oscillators working conditions) is an undistorted 3.3V CMOS 20MHz square wave at the inverters output and a clean 20MHz sine wave of 1V to 3V pk/pk (superimposed on the 1.65V bias point) at the inverters input. It is important the input waveform pk/pk value is always less than the inverters supply (Vdd) to prevent the input from limiting on the input protection diodes.

The actual Crystal power dissipation cannot be measured with an oscilloscope probe because the voltage across the crystal and current through the crystal are not in phase. This is caused by the designed load capacitance of 20pF requiring the crystal to be inductive (not resistive) at the working frequency. Assuming the actual crystal current could be measured (with a high bandwidth, ultra low inductance AC current probe for example) then there is still no way of determining the actual crystal power dissipation because the crystal 'resistance' in circuit is still not known. The crystal manufacturer will usually specify the maximum ESR (equivalent series resistance) and maximum Static Capacitance (C_0). In the above design these figures would be ~50Ω and ~7pF respectively. The actual ESR could be as low as 2Ω and Co as low as 1pF with more typical values being 15Ω and 3pF.

The equation for 'in circuit resistance' (R_e) is calculated as:-

$R_e = R_{esr} (1+ C_0/C_l)^2$

In our design C_l is the load capacitance of 20pF but R_{esr} and C_0 are unknowns unless they were measured on a specialised crystal impedance meter before the crystal was used in circuit.

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