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When mounting an oscillator circuit, the problem occasionally arises that, in addition to the well-known harmonics, the circuit produces more than the designed signal. If the possible operating frequency range of the used transistors is too large, the transistors will probably oscillate at additional higher frequencies due to parasitic effects such as pad capacitances of the circuit board or inductances of the connecting transmission lines. These generated additional signals at higher frequencies interfere with the projected oscillation frequency and with its harmonics and produce a number of disturbing spurious signals. The frequency spectrum of these additional signals mostly varies depending on the applied bias voltage and cannot be filtered straightforward by simple means because they are often too narrow to the desired signal. Hence, for a proper design of an oscillator circuit, the formation of such spurious signals must be suppressed right from the start by the help of precautionary circuit arrangement.

If the dimensions of the oscillator circuit are large enough, the engineer can try to solve the problem with the well-established approach of "cut and try." But the realization of the oscillator circuit in the SMD-technique leads to an awkward handling problem. A supplementary modification of the circuitry is completely impossible if the oscillator circuit is built as a

Oscillator Design for Suppressing Spurious Signals

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monolithic integrated circuit. Therefore, it is easier to use an adequate CAD program in time to avoid the problem of spurious signals.

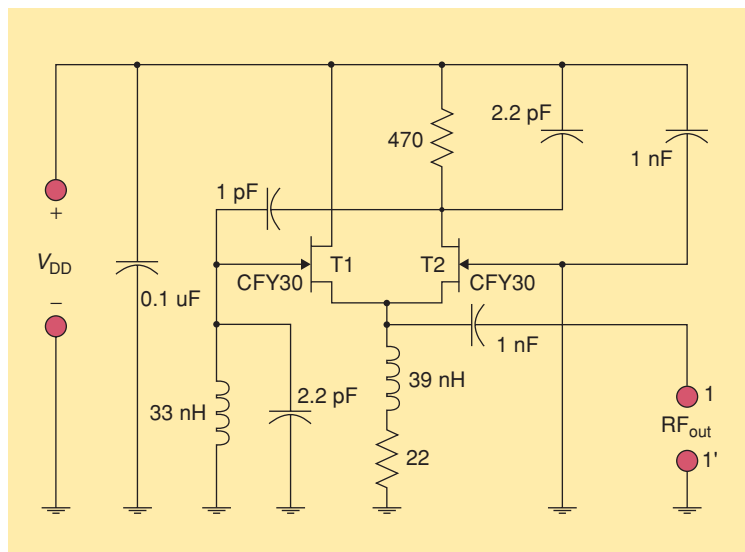


Figure 1. The circuit of the origin oscillator.

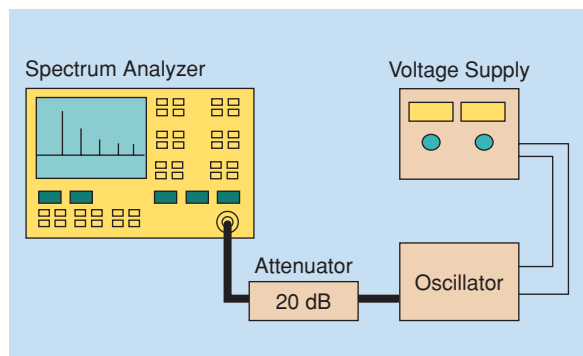


Figure 2. The measurement setup.

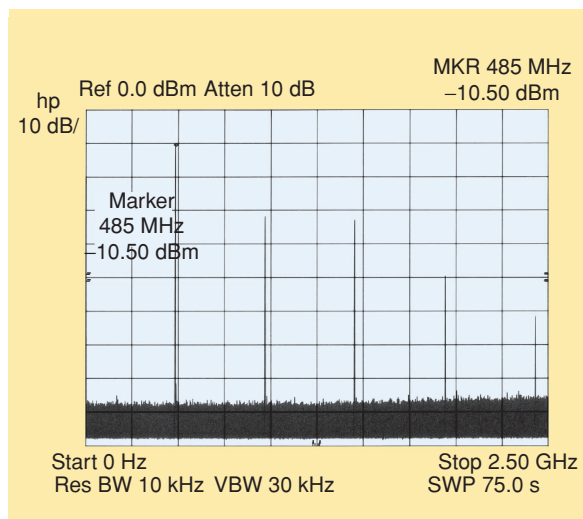


Figure 3. The spectrum from dc to 2.5 GHz of the origin oscillator at 1.7 Vdc.

The Oscillator Circuit

Within a research project, a simple oscillator circuit with an operating frequency of 480 MHz and an output power of at least 20 mW at a bias voltage in the range from 2–5 Vdc was needed. In a straightforward approach the circuitry published in [1] is used, which seems to be suitable for the requirements mentioned above. Although the circuit introduced in [1] delivers an output signal of just about 10 mW at 2 Vdc, there was a high degree of confidence for enhancing the output power by elevating the amount of the bias voltage. The circuit of the oscillator is given in Figure 1. The principle of the oscillator circuit is similar to the well-known Franklin oscillator [8]. The kernel of the oscillator uses two junction field-effect transistors (JFETs) as active devices and therefore has a high amplification factor. It can be regarded either as a source-coupled differential amplifier or as a two-stage amplifier in which the first stage is assembled with a JFET in a common-drain

configuration and the second stage is assembled with a JFET in common-gate circuit. In contrast to the Franklin oscillator, the parallel-tuned circuit is not isolated from the two-stage amplifier by means of small capacitors but rather by impedance matching. Further details of this oscillator circuit are already discussed extensive in [1]. The amplifier is both regenerative due to the feedback capacitor ($C_S = 1$ pF) and frequency selective due to a resonant circuit formed by an inductor ($L_R = 33$ nH) and a capacitor ($C_R = 2.2$ pF) connected, in parallel, to the inductor. When biasing the oscillator circuit, a very marginal amount of an alternating current at the resonant frequency is selected from the omnipresent noise and amplified by the two JFETs ($T_1 = \text{CFY30}$) and ($T_2 = \text{CFY30}$). The amplified signal is taken from the drain resistor ($R_D = 470 \Omega$) via the feedback capacitor ($C_S = 1$ pF) and filtered by the resonant circuit ($L_R = 33$ nH, $C_R = 2.2$ pF). Then the signal enters again the input port of the amplifier at the gate of the first JFET ($T_1 = \text{CFY30}$), and so on. The output signal (RF_{out}) is gathered directly from the source impedance ($Z_S = 22 \Omega + j\omega 39 \text{ nH}$) via the coupling capacitor ($C_O = 1$ nF). The impedance at this point is relatively low and already near to 50Ω . Therefore, an additional buffer amplifier is not necessarily required for proper operation. A further advantage of this oscillator circuit is that the input impedance at the gate of the first JFET ($T_1 = \text{CFY30}$) is relatively high. For this reason, the influence of the JFET's impedance on the loaded Q of the resonant circuit is low. The circuit arrangement was realized in SMD-technique on a small FR4 substrate. The problem arises when the mounted oscillator circuit was tested with a spectrum analyzer.

Measurements on the Origin Oscillator Circuit

The measurement setup is given in Figure 2. An attenuator with an attenuation factor of 20 dB was inserted between the oscillator circuit and the spectrum analyzer to avoid an input overload and to protect the measurement set up. An adjustable voltage source was used as the power supply. The measurement is started at a voltage of 1.7 Vdc. A part of results are given in Figure 3 for a frequency range from dc to 2.5 GHz. The spectrum shows the target frequency and its harmonics. Additional results to this measurement for a frequency range from 2.0–10 GHz are given in Figure 4 and show only the harmonics of the oscillator circuit. The spectrum is looking well, but the output power of the signal frequency is only 9.5 dBm at 1.7 Vdc. To increase the output power of the oscillator, the voltage source is adjusted to a higher amount of 2.8 Vdc. The measurement results are given in Figure 5 for a frequency range from dc to 2.5 GHz and in Figure 6 for a frequency range from 2.0–10 GHz

GHz. Although the output power at the operating frequency is increased up to 17.4 mW, the result is not satisfactory due to the high number of spurious oscillations excited. A further enhancement of the supply voltage to an amount of 3.9 Vdc finally leads to the wanted output power of 20 mW, but the spurious oscillations remain. The measurement results are given in Figure 7 for a frequency range from dc to 2.5 GHz and in Figure 8 for a frequency range from 2.0–10 GHz. When the supply voltage is increased to 5 Vdc, the output power of the oscillator at the designed frequency even becomes lesser and the spurious oscillations do not vanish. The measurement results are given in Figure 9 for a frequency range from dc to 2.5 GHz and in Figure 10 for a frequency range from 2.0–10 GHz. Now at the last, we had to use a suitable CAD program to analyze the problem.

CAD Analyzing of the Oscillator Circuit

To analyze the oscillator circuit, we use the CAD program C/NL2 from Maas [2]. There are a number of

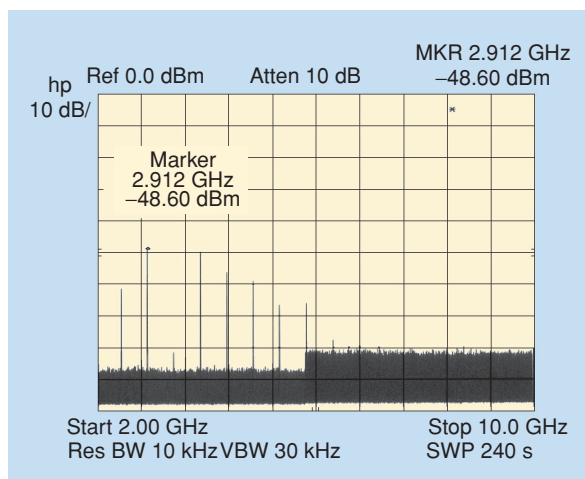


Figure 4. The spectrum from 2.0–10 GHz of the origin oscillator at 1.7 Vdc.

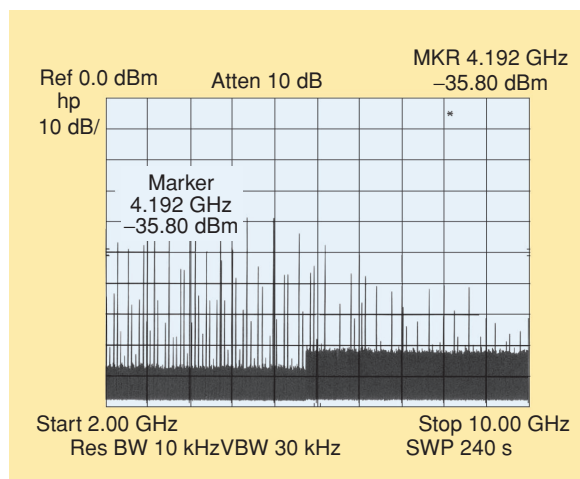


Figure 6. The spectrum from 2.0–10 GHz of the origin oscillator at 2.8 Vdc.

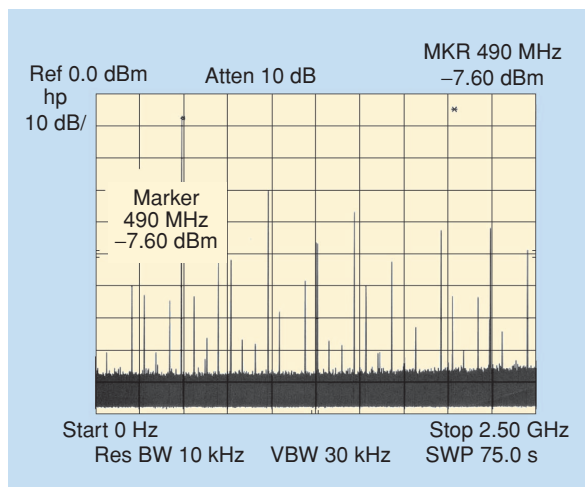


Figure 5. The spectrum from dc to 2.5 GHz of the origin oscillator at 2.8 Vdc.

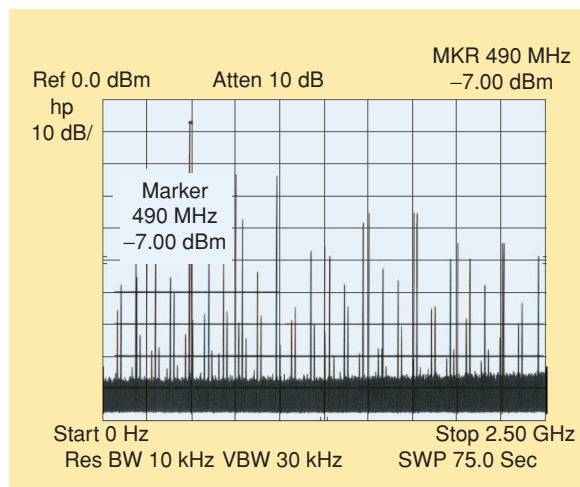


Figure 7. The spectrum from dc to 2.5 GHz of the origin oscillator at 3.9 Vdc.

other suitable CAD programs available for the RF engineer, and how they are used to solve the problem is

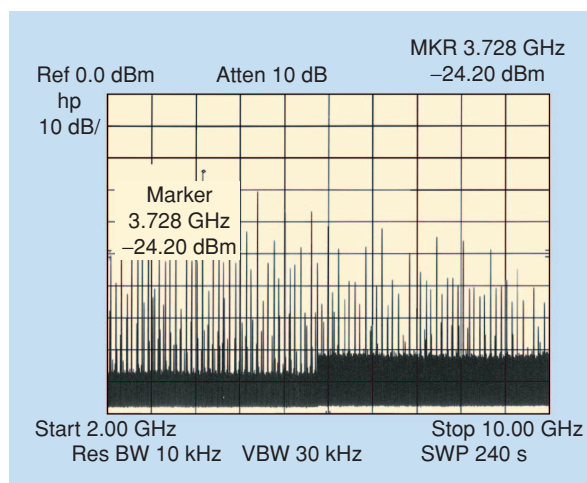


Figure 8. The spectrum from 2.0–10 GHz of the origin oscillator at 3.9 Vdc.

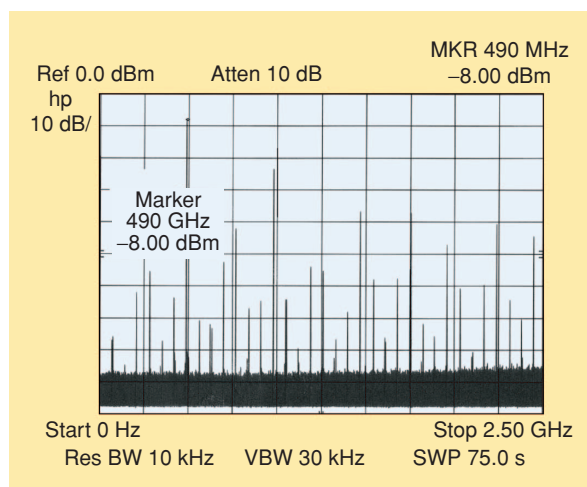


Figure 9. The spectrum from dc to 2.5 GHz of the origin oscillator at 5.0 Vdc.

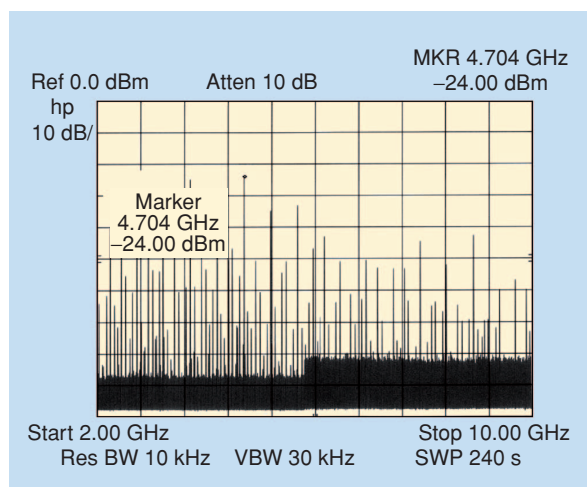


Figure 10. The spectrum from 2.0–10 GHz of the origin oscillator at 5.0 Vdc.

similar. Using other suitable CAD programs, sometimes one has to write a form of some additional sub-routines. In this article, however, the CAD program C/NL2 is used because it was at hand.

A detailed report of this program is given in a software review in [3]. Although this CAD tool is very compact and easy to use, it allows a very fast and effective implementation of all the necessary equations to calculate the voltage-dependent varying values of the intrinsic elements of both the JFETs during the tuning and analyzing sequence. Because this program was written primarily for a 486-machine, on a Pentium 4 computer it works much faster. Additionally, it is possible to insert a sufficient number of your own equations directly into the CAD program. That is why this fast and compact CAD program was preferred, until today. The program uses nodal analysis similar to SPICE. But that is no problem for an engineer.

The task is to determine the variation of small-signal parameters as a function of quiescent point and to predict the feasibility for oscillation. Remember, the JFETs used as active devices in this oscillator are the CFY30 from Infineon Technologies AG. From there, all results given in this article refers solely to this type of JFET, but results may be similar if comparable types are used.

The complete listing for the C/NL2 CAD program to analyze our oscillator circuit is given here.

After starting with the name of the file and first, the units are defined.

```

/*
  Oscillator Circuit *** Oscillator with
  APD ESB
*/
@ Define the units
UNITS
  freq = MHz
  Ind = nH
  cap = pF
  res = Ohm
  time = sec
END

Then, the frequency range of analysis from dc to
10 GHz in steps of 100 MHz is fixed and decided that at
this stage no noise analysis is necessary.

@ Define the frequency range from dc to
  10 GHz in steps of 100 MHz
FREQS
  0 10000 100
END
@ No, we are not interested in noise
analysis
MISC
  noise = false
END

```

To comfortably vary the amount of the supply voltage UB of the oscillator in the CAD program we have to declare it as a variable and to determine the range of variation. Here, the dc values from 1.5–5 Vdc should be run. The value is actually set to 3.5 Vdc.

```
@ Vdd varies from 1.5 Vdc to 5 Vdc
VAR
tvar UB 1.5 3.5 5
END
```

For describing the dc voltage dependence of the FETs used, we can now start with inserting our own equations. For this article, the N-channel GaAs JFETs of Type CFY30 with an ion-implanted planar structure in a SOT-143 package are used, which were at first produced by Siemens AG and afterward by Infineon Technologies AG. The characteristic electrical behavior of an oscillator circuit using JFETs as active devices typically depends significantly on the supply voltage. The main reason for this is the severe voltage dependence [4], [5] of the intrinsic transistor equivalent circuit elements, which represent the physical properties of the semiconductor substrate. To get a proper description of the nonlinear course of the characteristic parameters of the JFET's intrinsic equivalent circuit elements, a number of measurements for a wide range of appropriate values of the drain-source-voltage and the gate-source-voltage and for different values of the concerning resistors must be done [6], [7]. Then, the measured and calculated values are approximated by fast computable formulas. These equations are inserted here and produce a good forecast of the electrical behavior of the oscillator circuit with regard to the common operating voltage and the values of several necessary resistors in the oscillator circuit, which determine the different operating points of the active devices, respectively. The dc circuit is shown in Figure 11 [6] and clarifies the physical context of the dc quantities. Due to the voltage drop (V_r) at the drain resistor (R_D), the dc values of the two drain-source-voltages (V_{ds1}) and (V_{ds2}) are always different, whereas those of the two gate-source-voltages (V_{gs1}) and (V_{gs2}) are always the same. The relevant values of the dc quantities depend on the supply voltage (V_C), the two resistors (R_D) and (R_S), and the electrical characteristics of the JFETs used. To determine the context of the particular values of the prevailing dc quantities, an adequate number of measurements had to be done with varying values of the supply voltage (V_C) and the two resistors (R_D , R_S), respectively [7]. The details of the measurement setup and the approximation formulas are given in [6] and [7]. For completeness, some fundamental formulas from [6], using a proven curve fitting method [13] to obtain fast computable approximation formulas from the measured values, are repeated here. The dependence of the value of the first JFET's (T_1) drain-source-voltage (V_{ds1} , see Figure 11)

from the supply voltage (V_C) and the source resistor (R_S) is given by

$$\frac{V_{ds1}}{V} = 0.9613 \frac{V_C}{V} - \left[1.0246 \left(1 - e^{-f_{01}} \right) \times \left(1 - e^{-f_{02}} \right) \right] \quad (1)$$

with the abbreviations

$$f_{01} = 0.0303 \frac{R_S}{\Omega} \quad (2)$$

and

$$f_{02} = 1.385 \frac{V_C}{V}. \quad (3)$$

After performing the curve fitting method mentioned above, the following approximation formula is describing the value of the second JFET's (T_2) drain-source-voltage (V_{ds2}) as a function of the supply voltage (V_C), the drain resistor (R_D) and the source resistor (R_S). It is given by

$$\frac{V_{ds2}}{V} = \frac{V_{ds1}}{V} e^{-\frac{R_D}{\Omega}} + f_{03} \left(1 - e^{-\frac{R_D}{\Omega}} \right) \quad (4)$$

with the abbreviations

$$f_{03} = 0.6884 \frac{V_C}{V} \left(1 - e^{-f_{04}} \right) \quad (5)$$

and

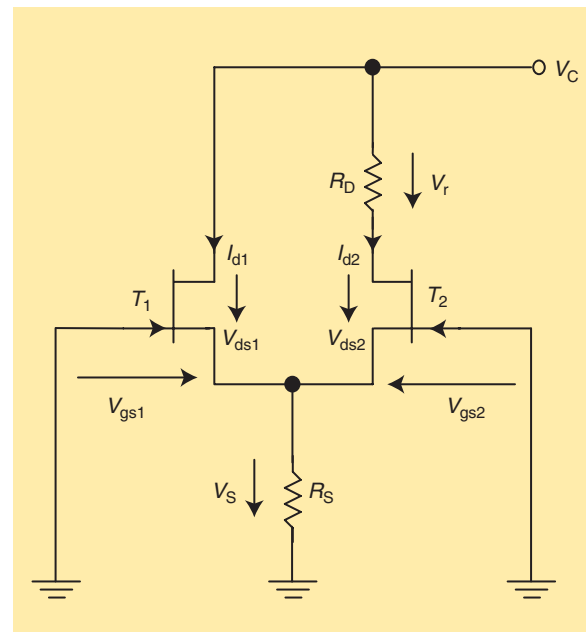


Figure 11. The context of the dc quantities.

$$f_{04} = 8.918 \left(\frac{R_D}{\Omega} \right)^{-1.14} \left(\frac{R_S}{\Omega} \right)^{0.4815} \frac{V_C}{V}. \quad (6)$$

In the C/NL2 CAD program, these equations are inserted easily. First the relevant resistors, the drain resistor (R_D) and the source resistor (R_S) must be specified.

```
@ Here we insert our own equations
EQNS
@ We must specify the actually used
  source- and drain-resistors
  Rs = 22
  Rd = 470
@ Now the actual drain-source voltages
  of both JFETs are calculated
  Uds1 = 0.9613*Ub-(1.0246*(1.-exp
    (-0.0303*Rs))*(1.-exp
    (-1.385*Ub)))
  Uds2 = Uds1*exp(-Rd)+0.6884*Ub* (1.-
    exp(-Rd))*(1.-exp(-8.918*Ub
    *exp(-1.14*log(Rd))
    *exp(0.4815*log(Rs))))
@ Both gate-source-voltages are the same
  Ugs = Uds1 - Ub
```

After calculating the dc quantities, now the voltage dependent equivalent circuit elements of the JFETs have to be calculated. Figure 12 shows the complete equivalent circuit of the JFET with its intrinsic voltage dependent elements. The equivalent circuit of the CFY30 has a number of elements, which are not affected by the actual voltages, representing for example bonding wires and housing capacities. The details of the determination of the variation of small-signal parameters as a function of dc operating point and the approximation formulas are given in [6] and [7].

A very large number of further suitable equivalent circuit models are already established [16]–[28]. All of them are meaningful especially in the particular physical context for which they are used. The empirical models also use curve-fitting functions like polynomials and cubic splines.

Here, fitting functions are used for representing the bias dependencies of the intrinsic elements. The same technique is utilized as described in conjunction with the modeling of the nonlinear dependence of the dc quantities from the values of the circuit elements and the bias voltage. This does not mean that this method claims to be the best one. The decision for this procedure was reached because some well-processed computer programs previously used for a thesis [13] were still on hand. The complete sets of S-parameters of a typical CFY 30 were measured with a network analyzer in the frequency range from 40 MHz to 26 GHz at a drain-source-voltage varying from 0.25–5.0 Vdc in steps of 0.25 Vdc and a gate-source-voltage varying

from 0.0–1.4 Vdc in steps of 0.2 Vdc, respectively [7]. The voltage steps are relatively large, and that is why the model gets interpolated during simulation. Of course, this will result in a reduced accuracy of the model. On the other hand, the number of data must be limited. Thus, the number and magnitude of the voltage steps used seem to be an acceptable compromise between the required accuracy and the expenditure of measurements and time.

A suitable CAD program [2] has been used for fitting these measured data sets to the S-parameters of the equivalent circuit, which is necessary to model the JFETs. The circuit-element values are altered as long as the error between the calculated S-parameters of the model and the measured S-parameters of the physical device becomes infinitesimal. Then, the nonlinear shapes of the characteristics of the intrinsic transistor equivalent circuit elements are approximated by some fast computable formulas. To obtain these expressions with a curve-fitting procedure already mentioned [13], the maximum error between the values of the equivalent circuit elements and those obtained by the formulas is stipulated to about 5%. For completeness reasons, some fundamental formulas from [6] and [7], using a proven curve fitting method [13] to obtain fast computable approximation formulas from the measured values, are repeated here. The calculation formula for the transconductance (g_m), depending on both the drain-source-voltage (V_{ds}) and the gate-source-voltage (V_{gs}) is given by

$$\frac{g_m}{mS} = f_{05} (1 - e^{-f_{06}}) + f_{07} e^{-f_{08}}, \quad (7)$$

with the abbreviations

$$f_{05} = 46.5108 + 17.2463 \frac{V_{gs}}{V}, \quad (8)$$

$$f_{06} = \left(1.6208 + 1.013 \frac{V_{gs}}{V} \right) \frac{V_{ds}}{V}, \quad (9)$$

$$f_{07} = 54.7903 + 30.1191 \frac{V_{gs}}{V} \quad (10)$$

and

$$f_{08} = \left(1.1292 + 0.4028 \frac{V_{gs}}{V} \right) \frac{V_{ds}}{V}. \quad (11)$$

The value of the intrinsic gate-source-resistor (R_{gs}) is found to be nearly independent on both the drain-source-voltage (V_{ds}) and the gate-source-voltage (V_{gs}). This intrinsic element describes predominantly the losses in the gate structure of the semiconductor substrate. Obviously, the losses depend more on details of the technologically realized physical structure than on the bias voltages. Due to the very slight dependence found at the type of JFET examined here,

z the intrinsic gate-source-resistor (R_{gs}) is assumed to be constant. Within an arising maximum error between the values of the equivalent circuit elements and those calculated by the approximation formulas, which is arbitrary determined to be about 5%, the value of the intrinsic gate-source-resistor (R_{gs}) can be fixed to be 13.3Ω .

The calculation formula for the intrinsic drain-source-resistor (R_{ds}), depending on both the drain-source-voltage (V_{ds}) and the gate-source-voltage (V_{gs}) is given by

$$\frac{R_{ds}}{\Omega} = (1 - e^{-f_{09}}) \left(61.9328 \frac{V_{ds}}{V} + f_{10} \right) \quad (12)$$

with the abbreviations

$$f_{09} = 18.8152 \frac{V_{ds}}{V} \quad (13)$$

and

$$f_{10} = \frac{48.0917}{\frac{V_{gs}}{V} + 1.5725} \quad (14)$$

The calculation formula for the intrinsic drain-source-capacitor (C_{ds}), depending on both the drain-source-voltage (V_{ds}) and the gate-source-voltage (V_{gs}) is given by

$$\frac{C_{ds}}{fF} = 285.732 (1 - e^{-f_{11}}) - 31.60106 \quad (15)$$

with the abbreviation

$$f_{11} = \frac{1.1569}{\frac{V_{gs}}{V} + 1.483} \frac{V_{ds}}{V} \quad (16)$$

The calculation formula for the intrinsic gate-drain-capacitor (C_{gd}), depending on both the drain-source voltage (V_{ds}) and the gate-source voltage (V_{gs}) is described by

$$\frac{C_{gd}}{fF} = 68.6765 \left(\frac{V_{gs}}{V} + 2.7009 \right) e^{-f_{12}} + 32.2529 \quad (17)$$

with the abbreviation

$$f_{12} = \frac{1.2787}{1.1337 + \left(\frac{V_{gs}}{V} \right)^2} \frac{V_{ds}}{V} \quad (18)$$

The calculation formula for the intrinsic gate-source capacitor (C_{gs}), depending on both the drain-source voltage (V_{ds}) and the gate-source voltage (V_{gs}) is obtained as

$$\frac{C_{gs}}{fF} = f_{13} \left(1 - \frac{1.5902 \cdot e^{-f_{14} \frac{V_{ds}}{V}}}{1 + e^{-f_{15} \frac{V_{ds}}{V}}} \right) + f_{16} \quad (19)$$

with the abbreviations

$$f_{13} = 74.0671 \frac{V_{gs}}{V} + 250.2, \quad (20)$$

$$f_{14} = 0.0085 \frac{V_{gs}}{V} + 0.4944, \quad (21)$$

$$f_{15} = 0.4895 \frac{V_{gs}}{V} + 1.7453 \quad (22)$$

and

$$f_{16} = 148.371 \frac{V_{gs}}{V} + 494.613. \quad (23)$$

Now, the equations necessary for the proper calculation of the oscillator circuit can be completed. One has to apply the formulas two times for each JFET individually, because they have different quiescent points. Note that the formula for the transconductance is in [mS] whereas the units in the CAD program are [S].

```
@ JFET 1
gm1 = (0.0465108+0.0172463*Ugs)
      *(1.-exp(-1.6208-1.0130*Ugs)
      *Uds1)+(0.0547903+0.0301191
      *Ugs) *exp(-1.1292-0.4028*Ugs)
      *Uds1
rds1 = (1.-exp(-18.8152*Uds1))
      *(61.9328*Uds1+48.0917/
      (Ugs+1.5725))
cds1 = 0.285732*(1.-exp(-1.1569
      *Uds1/(Ugs+1.483)))-
      0.03160106
cgd1 = 0.001*((68,6765*(Ugs+2.7009)
      *exp(-1.2787*Uds1/(1.1337
      +Ugs*Ugs)))+32.2529)
gs1a = 1.+exp(-Uds1*(0.4895*Ugs
      +1.7453))
cgs1 = (0.0740671*Ugs+0.2502)
      *(1.-1.5902*exp(-Uds1*
      (0.0085*Ugs+0.4944))/gs1a)
      +(0.148371*Ugs+0.494613)

@ JFET 2
gm2 = (0.0465108+0.0172463*Ugs)
      *(1.-exp(-1.6208-1.0130*Ugs)
      *Uds2)+(0.0547903+0.0301191*Ug
      s) *exp(-1.1292-0.4028*Ugs)
      *Uds2
rds2 = (1.-exp(-18.8152*Uds2))
      *(61.9328*Uds2+48.0917/(Ugs
      +1.5725))
```



```

cds2 = 0.285732*(1.-exp(-1.1569
*Uds2/(Ugs+1.483)))-
0.03160106
cgd2 = 0.001*( (68,6765*(Ugs+2.7009)
*exp(-1.2787*Uds2/(1.1337
+Ugs*Ugs)))+32.2529)
gs2a = 1.+exp(-Uds2*(0.4895*Ugs
+1.7453))
cgs2 = (0.0740671*Ugs+0.2502)*(1.-
1.5902*exp(-Uds2*(0.0085
*Ugs+0.4944))/gs2a)
+(0.148371*Ugs+0.494613)
END

```

This completes the equation section of the C/NL2 CAD program. Now, the voltage-dependent oscillator circuit can very accurately be described. Because we were to sluggard to read the C/NL2 handbook properly, we will treat the oscillator circuit as a two port, with a signal port (node 51) and with a second dummy port (node 99), just loaded by 50 Ω . The oscillator circuit is called "osc," and both ports are terminated with 50 Ω each. The node 0 denotes the ground.

```

CKT osc 51 99
Rs 51 0 50
Rl 99 0 50

```

At this stage, both of the JFETs with all their intrinsic voltage-dependent elements can be described. For the first JFET, we connect the gate of with node 1, the drain with node 11, and the source with node 50. For the second JFET we connect the gate of with node 21, the drain with node 31, and the source with node 50. Note that both sources are directly connected together in the oscillator circuit. The transmission lines given in Figure 12 are extremely short and have no influence on the measured data. Therefore they are neglected in the equivalent circuit calculated by the C/NL2 CAD program.

```

@ First JFET node 1: gate node 11:
drain node 50: source
IND 1 3 0.926
CAP 1 50 0.022
RES 3 4 6.4
CAP 4 5 cgs1
RES 5 6 13.3
VCCS 4 5 8 6 gml
1.5E-12 1.0E-12
CAP 8 6 cds1
RES 8 6 rds1
IND 6 7 0.0138
RES 7 50 5.4
CAP 4 8 cgd1
RES 8 9 6.3
IND 9 11 0.981
CAP 11 50 0.039
CAP 1 11 0.0063

```

```

@ Second JFET node 21: gate node 31:
drain node 50: source
IND 21 23 0.926
CAP 21 50 0.022
RES 23 24 6.4
CAP 24 25 cgs2
RES 25 26 13.3
VCCS 24 25 28 26 gm2
1.5E-12 1.0E-12
CAP 28 26 cds2
RES 28 26 rds2
IND 26 27 0.0138
RES 27 50 5.4
CAP 24 28 cgd2
RES 28 29 6.3
IND 29 31 0.981
CAP 31 50 0.039
CAP 21 31 0.0063

```

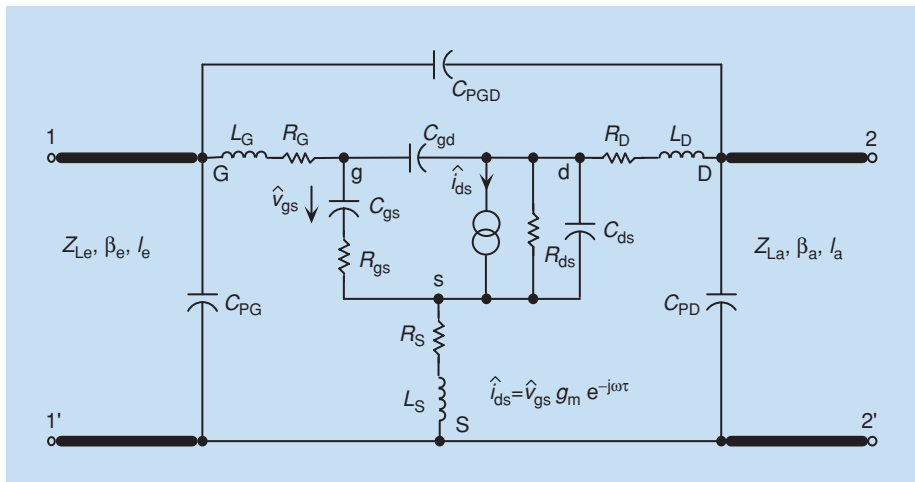


Figure 12. The complete equivalent circuit of the JFET with intrinsic voltage-dependent elements.

We have described the voltage-dependent active kernel of the oscillator. Now, the special oscillator circuit must be implemented. Note that for small signal purposes it is the same, whether we connect a node to ground (node 0) or to Vdd, because the supply voltage is shorted by a large capacitor. Remember that the node 99 just defines a dummy port. The wires to ground are simulated as resistors with 0 Ω .

```

@ Drain (node "21") JFET 1 to Vdd (same
as ground)
RES 21 0 0.0
@ Gate (node "11") JFET2 to ground
RES 11 0 0.0
@ Drain (node "31") JFET2 over Rd to Vdd
(same as ground)
RES 31 0 470
@ Rd is shunted by a capacitor
CAP 31 0 2.2
@ Gate (node "1") JFET 1 has parallel
resonant circuit
CAP 1 0 2.2
IND 1 0 33.0
@ Feedback capacitor between Gate ("1")
JFET1 and Drain ("31") JFET2
CAP 1 31 1.0
@ Source (node"50") impedance to ground
("0")
IND 50 59 39
RES 59 0 22
@ Output coupling capacitor to port 1
(node "51")
CAP 50 51 1000
@ Just a loaded dummy port (node "99"),
don't care for it....
RES 99 0 50
END

```

Finally, it has to be defined what the output section of the CAD program should contain. We are just interested in the magnitude of the reflection coefficient s_{11} in decibels.

```

OUT
      osc    db[s11]      scn
END

```

Now, the C/NL2 CAD program is ready to analyze the problem. It is a comfortable tool to find out the reasons for the additional oscillations and to find a means to avoid them without tuning the small SMD circuitry by replacing the components with the soldering iron.

First, we have to try to simulate additional oscillations. For a really proper calculation and an accurate simulation of the electrical behavior of the oscillator circuit, the parasitic elements of the used SMD components [29] and all further existing components influencing the electrical characteristics of the oscillator circuit should be taken into account. Even the etched contact pad's parasitic capacitances to the ground and the parasitic inductance of the via-holes to the ground may not be neglected. Therefore, an exact prediction of these effects can only be carried out, if the relevant parasitic elements are considered sufficiently [7].

To save time we tried to shorten the procedure and just searched for a rough description of the principle problem.

An inspection of the SMD layout by a microscope shows some connection transmission lines between the pads, which seem to be a little bit too thin. Obviously this is due to an undercut caused by too long chemical etching during the production process. We assumed the parasitic inductance of such a connection transmission line to be about 1 nH. To save the time, only this single parasitic element was taken into account and all the other possible ones were ignored. So, an additional inductance of 1 nH was inserted between the gate of the first JFET and the resonant circuit. For this reason an additional node (55) had to be introduced. This yields a modified program listing.

```

@ Gate (node "1") JFET 1 has parallel
resonant circuit
@ Gate (node "1") JFET1 has additional
parasitic inductance of 1 nH
IND 1 55 1.0
CAP 55 0 2.2
IND 55 0 33.0

```

The simulated [7] amount $|s_{11}|$ of the complex S-parameter s_{11} is considered for a wide frequency range from dc up to 10 GHz. The analysis of the modified oscillator circuit gives three additional facilities for additional oscillations in the upper gigahertz region. This seems to be the reason for the spurious oscillation. Figure 13 shows the course of the magnitude of the reflection coefficient s_{11} from dc to 10 GHz.

The frequency dependent course of the simulated amount $|s_{11}|$ of the complex S-parameter s_{11} shows four significant peaks. The simulation indicates that the oscillator is able to generate at least four RF signals at different frequencies at the same time. The RF signal at a frequency of 480 MHz obviously depends on the values of the resonant circuit (L_R , C_R). The RF signals at frequencies of 5.0, 7.0, and 10.0 GHz seems to depend on the values of the parasitic circuit elements [29], [30]. All the simulated individual oscillations are

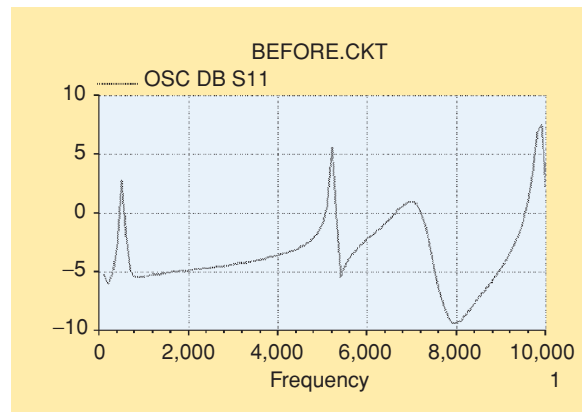


Figure 13. The course of the magnitude of the reflection coefficient s_{11} from dc to 10 GHz, indicating a number of additional oscillations.

independent from each other. The computer simulation shows that the lower frequency peak remains unchanged and all the upper frequency peaks vanish if the parasitic inductive element is neglected. On the other hand, the lower frequency peak vanishes and the upper frequency peaks remains unchanged if the resonant circuit is taken away in the simulation. So, there are obviously different physical reasons for each oscillation condition. Therefore they are able to exist at the same time.

An oscillator circuit converts the direct current energy of a battery or a power supply into a continuously alternating current at a specific frequency. After all, an oscillator circuit simply represents a selective regenerative amplifier for one single frequency. A very marginal amount of an alternating current at this specific frequency is selected from the omnipresent noise, generated for instance by the active devices and is amplified by the oscillator circuit as long as the amplitude is sufficient.

To limit the amplitude of the continuously alternating current at a specific frequency the amplification characteristic of the oscillator must be nonlinear [9], [10], that is, the amplification must shrink with increasing amplitude.

A very easy and comfortable procedure to ascertain the condition for oscillation is to calculate the frequency dependent amount $|\underline{s}_{11}|$ of the complex S-parameter \underline{s}_{11} at the output port (RF_{out}) of the oscillator circuit [11], [12] with the help of a suitable CAD tool [2].

If the amount of this reflection coefficient is less than one at the prevailing frequency, the oscillator remains passive and will not produce any RF signals.

However, if the amount of the reflection coefficient is significantly larger than one, the oscillator becomes an active device and will start to oscillate at the target frequency. It should be emphasized that this procedure solely predicts the low-signal condition for oscillation. For instance, the frequency drift due to the generated signals influence on the intrinsic elements or the amount of the generated output power cannot be determined by this procedure.

To determine solely the oscillation condition of an oscillator circuit, we have to contemplate the electrical behavior at a very low amplitude level since the oscillator must at first start to generate an alternating current at a specific frequency. For this reason it is sufficient to consider only the oscillators small signal inherent reflection factor as a first step. The frequency drift caused by too large amplitudes of the generated signal or the problems with distortion of the sinusoidal curves and the resulting harmonics are not considered here.

Therefore, to determine whether or not a circuit will operate as an oscillator, a very elementary criterion is used. For a passive electrical one-port the amount of the frequency dependent inherent reflection

factor is always less or equal to one. If it is significantly larger than one at a specific frequency this will indicate, that the one-port generates audio or radio frequency power, there.

Mixture of Spectral Lines

To give some explanation for the number of the resulting spectral lines, we regard the simple mixture of two sinusoidal voltages $u1(t)$ and $u2(t)$ with different frequencies $f1$ and $f2$. The nonlinear context between the current $i(t)$ and the signal voltage $u(t)$ at an active element can be described approximately by a polynomial with the order of n , where $k1$ until kN are general coefficients [7]

$$i(t) = k1 \cdot u(t) + k2 \cdot u^2(t) + k3 \cdot u^3(t) + \dots + kN \cdot u^N(t). \quad (23)$$

If the signal voltage $u(t)$ is a superposition of two sinusoidal voltages with different frequencies and different amplitudes, it can be written

$$u(t) = u1(t) + u2(t) \quad (24)$$

with

$$u1(t) = U1 \cdot \sin(2 \cdot \Pi \cdot f1 \cdot t) \quad (25)$$

and

$$u2(t) = U2 \cdot \sin(2 \cdot \Pi \cdot f2 \cdot t). \quad (26)$$

After inserting (24) into (23) and assuming a polynomial order of only $N = 4$, then the following result may be obtained:

$$\begin{aligned} i(t) = & k1 \cdot U1 \cdot \sin(2 \cdot \Pi \cdot f1 \cdot t) + k1 \cdot U2 \\ & \cdot \sin(2 \cdot \Pi \cdot f2 \cdot t) + k2 \cdot U1^2 \\ & \cdot \sin^2(2 \cdot \Pi \cdot f1 \cdot t) + k2 \cdot U2^2 \\ & \cdot \sin^2(2 \cdot \Pi \cdot f2 \cdot t) + 2 \cdot k2 \cdot U1 \cdot U2 \\ & \cdot \sin(2 \cdot \Pi \cdot f1 \cdot t) \cdot \sin(2 \cdot \Pi \cdot f2 \cdot t) \\ & + k3 \cdot U1^3 \cdot \sin^3(2 \cdot \Pi \cdot f1 \cdot t) \\ & + k3 \cdot U2^3 \cdot \sin^3(2 \cdot \Pi \cdot f2 \cdot t) \\ & + 3 \cdot k3 \cdot U1^2 \cdot U2 \cdot \sin^2(2 \cdot \Pi \cdot f1 \cdot t) \\ & \cdot \sin(2 \cdot \Pi \cdot f2 \cdot t) + 3 \cdot k3 \cdot U1 \cdot U2^2 \\ & \cdot \sin(2 \cdot \Pi \cdot f1 \cdot t) \cdot \sin^2(2 \cdot \Pi \cdot f2 \cdot t) \\ & + k4 \cdot U1^4 \cdot \sin^4(2 \cdot \Pi \cdot f1 \cdot t) \\ & + k4 \cdot U2^4 \cdot \sin^4(2 \cdot \Pi \cdot f2 \cdot t) \\ & + 4 \cdot k4 \cdot U1^3 \cdot U2 \cdot \sin^3(2 \cdot \Pi \cdot f1 \cdot t) \\ & \cdot \sin(2 \cdot \Pi \cdot f2 \cdot t) + 4 \cdot k4 \cdot U1 \cdot U2^3 \\ & \cdot \sin(2 \cdot \Pi \cdot f1 \cdot t) \cdot \sin^3(2 \cdot \Pi \cdot f2 \cdot t) \\ & + 6 \cdot k4 \cdot U1^2 \cdot U2^2 \cdot \sin^2(2 \cdot \Pi \cdot f1 \cdot t) \\ & \cdot \sin^2(2 \cdot \Pi \cdot f2 \cdot t) \end{aligned} \quad (27)$$

In this expression the following frequency combinations are appearing:

- 1) the two frequencies f_1 and f_2
- 2) the harmonics $2 * f_1$, $3 * f_1$, $4 * f_1$, $2 * f_2$, $3 * f_2$ and $4 * f_2$
- 3) the mixtures of second grade $f_1 \pm f_2$
- 4) the mixtures of third grade $2 * f_1 \pm f_2$ and $f_1 \pm 2 * f_2$
- 5) the mixtures of fourth grade $3 * f_1 \pm f_2$, $2 * f_1 \pm 2 * f_2$, $f_1 \pm 3 * f_2$.

These are already the resulting frequencies, if N just to be four is assumed. More realistic is an amount of N of above 18, but to calculate it is beyond the our scope. However, (27) gives a good impression of the properties and explains the high number of spectral lines due to spurious oscillations.

On the other hand, the numerous oscillations are enabled by one and the same kernel with two JFETs. The first oscillation at a frequency of 480 MHz generates harmonics up to a frequency of at least 10 GHz (see Figure

15). At the same time, the other oscillations at a frequency of 5.0, 7, and 10 GHz also generate harmonics, too. Due to the nonlinear characteristic of the JFETs, all these signals mix with each other, producing a large number of additional spectral lines, which are called spurious oscillations. Note that the amplitudes of the harmonics decrease with increasing frequency, whereas the amplitudes of the spurious oscillations decrease with decreasing frequency. This is due to the mixing process. When measuring the oscillator's spectrum with the spectrum analyzer, a slight variation of the supply voltage of the assembled oscillator causes the spurious oscillations to shift, whereas the 480 MHz signal and its harmonics are very stable. This is due to the fact that the influence of the voltage dependent intrinsic elements on the higher frequency oscillations is relatively large. So the mixed down spurious oscillations are directly affected by the supply voltage, whereas the 480 MHz signal is primarily determined by the values of the resonant circuit elements, which are completely independent from the supply voltage.

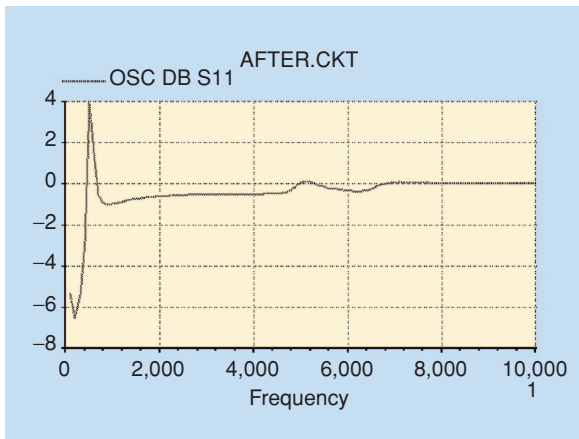


Figure 14. The course of the magnitude of the reflection coefficient s_{11} from dc to 10 GHz, indicating the suppression of additional oscillations.

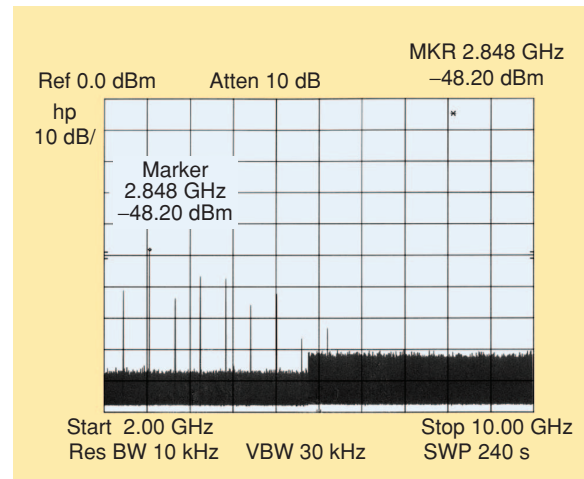


Figure 16. The spectrum from 2.0–10 GHz of the improved oscillator at 1.7 Vdc.

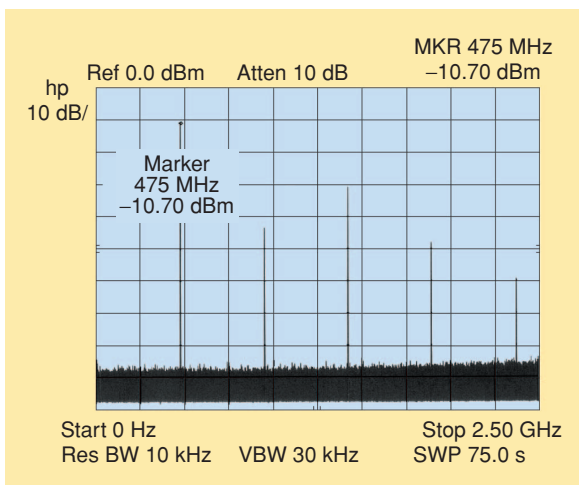


Figure 15. The spectrum from dc to 2.5 GHz of the improved oscillator at 1.7 Vdc.

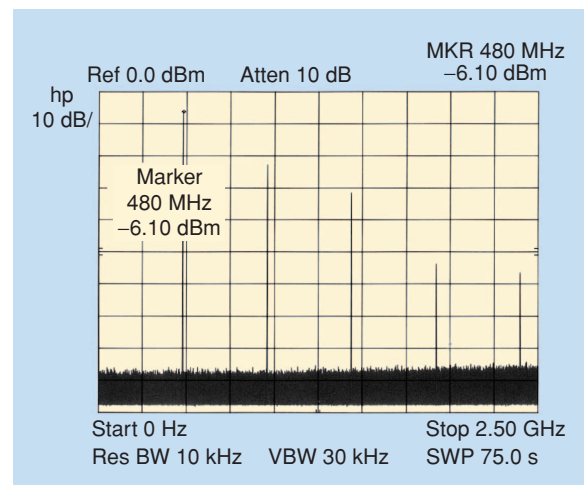


Figure 17. The spectrum from dc to 2.5 GHz of the improved oscillator at 2.8 Vdc.

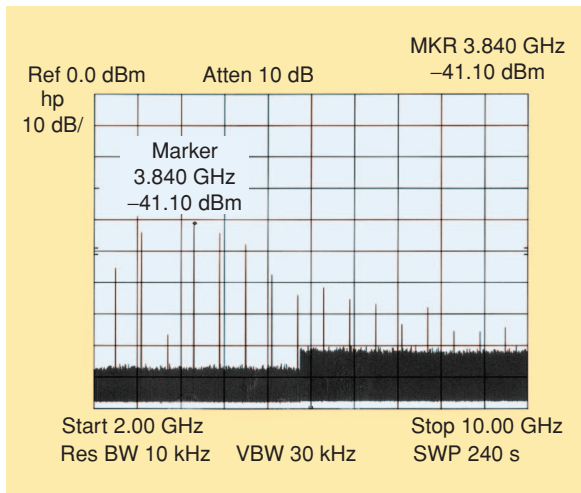


Figure 18. The spectrum from 2.0–10 GHz of the improved oscillator at 2.8 Vdc.

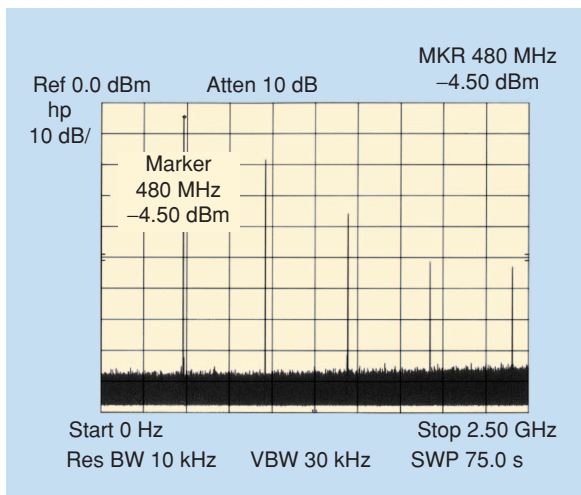


Figure 19. The spectrum from dc to 2.5 GHz of the improved oscillator at 3.9 Vdc.

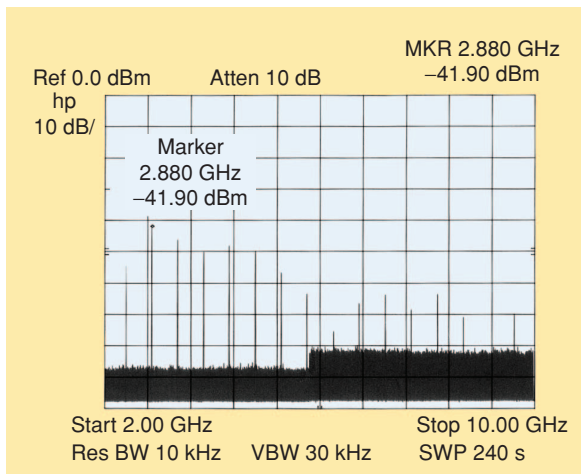


Figure 20. The spectrum from 2.0–10 GHz of the improved oscillator at 3.9 Vdc.

CAD Improving of the Oscillator Circuit

Now the circuit of the oscillator simulated can easily be modified by the computer program C/NL2 to find an effective means to suppress the additional oscillations.

It is sometimes the same procedure as the common “cut and try” technique, but one needs no soldering iron and must not always go into the laboratory and connect the device to the measuring setup. During the experiments performed here, many possible modifications of the oscillator circuit at a number of different assumed supply voltages were tested.

The values of the involved resistors, inductors, and capacitors are varied. Additional resistors, inductors, and capacitors are introduced into the circuit or the already existing ones are replaced. After each modification the frequency dependent amount $|\underline{s}_{11}|$ of the complex S-parameter \underline{s}_{11} at the output port (RF_{out}) of the oscillator circuit was calculated to be able to decide whether or not the modification is an improvement. At first, some disappointment is observed. Either the effect on the spurious oscillations was not effective enough or the desired signal itself was suppressed too much.

Finally, we found a very simple answer to the spurious oscillation problem of our oscillator. C/NL2 indicates by calculating the frequency dependent amount $|\underline{s}_{11}|$ of the complex S-parameter \underline{s}_{11} at the output port (RF_{out}) of the oscillator circuit that it is absolutely sufficient to insert an additional capacitor in parallel to the oscillator’s output port (compare Figures 1 and 23). This will suppress all higher frequency oscillations without affecting the desired oscillation frequency.

Figure 14 shows the result of the simulation with an assumed value of the additional capacitor of 10 pF. The value of the capacitor was chosen relatively high during the CAD-modification of the oscillator circuit to produce a significant effect. When realizing the modification on our SMD circuitry with the help of a soldering-iron, we later found a value of 3.3 pF to be completely sufficient.

To explain this circuit fix, we have to speculate a little bit about the physical reasons. The circuitry is too complex for just a simple answer. From earlier investigations we know that the number of additional oscillations may be less if another combination of the values of the resistor and the inductor which form the source impedance ($Z_S = 22 \Omega + j\omega 39 \text{ nH}$) is used.

So, the source impedance seems to affect significantly the high frequency behavior of the oscillator circuit. This is due to the fact that the currents of both the FETs are galvanically coupled in this special oscillator circuit. With the combination we used here, however, we have even three additional unwanted oscillations at higher frequencies.

What all these disturbing additional oscillations have in common here is that their frequency range is much higher than the frequency of the desired oscillation. By introducing an additional capacitor in parallel

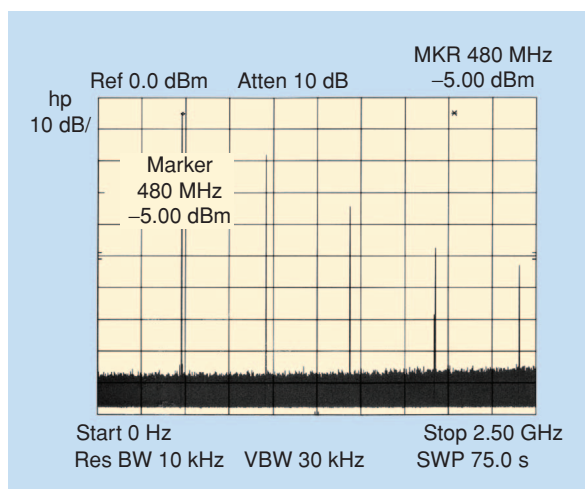


Figure 21. The spectrum from dc to 2.5 GHz of the improved oscillator at 5.0 Vdc.

to the oscillator's output port, this capacitor almost shortens the source Impedance relating to the unwanted high frequency oscillations.

For these high frequencies, the two transistor used seem to be not coupled with each other due to the additional capacitor and therefore the high frequency oscillation is suppressed.

Results

After inserting an additional capacitor with a value of 3.3 pF, the measurement of the improved oscillator circuit was started at a voltage of 1.7 Vdc. The measurement results are given in Figure 15 for a frequency range from dc to 2.5 GHz. The spectrum shows the intended frequency and its harmonics. The measurement results for a frequency range from 2.0–10 GHz are given in Figure 16 and show only the harmonics of the oscillator circuit. In principle, there is hardly any difference to the corresponding figures of the origin oscillator, namely Figures 3 and 4.

To increase the output power of the oscillator, the voltage source is adjusted to a higher amount of 2.8 Vdc. Now, the exciting question was whether there will be spurious oscillations or not. The measurement results are given in Figure 17 for a frequency range from dc to 2.5 GHz and in Figure 18 for a frequency range from 2.0–10 GHz. No spurious oscillations could be measured. Only the intended

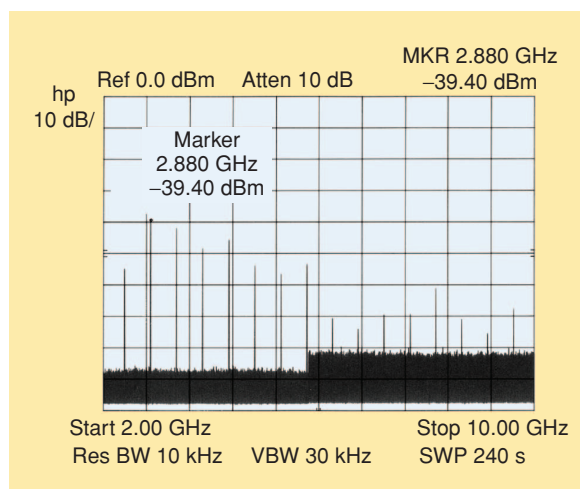


Figure 22. The spectrum from 2.0–10 GHz of the improved oscillator at 5.0 Vdc.

frequency and its harmonics could be measured. What a difference to the corresponding figures of the origin oscillator, namely Figures 5 and 6. In addition, the measured output power at 480 MHz is about 25 mW. So, we completely reached our design goal with very simple means.

Next, it was asked, what will happen if the amount of the supply voltage will be further increased. So the testing procedure of the improved oscillator circuit was started. An increasing of the supply voltage to an amount of 3.9 Vdc finally leads to an output power of 35 mW. The measurement results are given in Figure 19 for a frequency range from dc to 2.5 GHz and in Figure 20 for a frequency range from 2.0–10 GHz. Even if the supply voltage is increased to 5 Vdc, no spurious oscillations could be detected. Only the output power of the

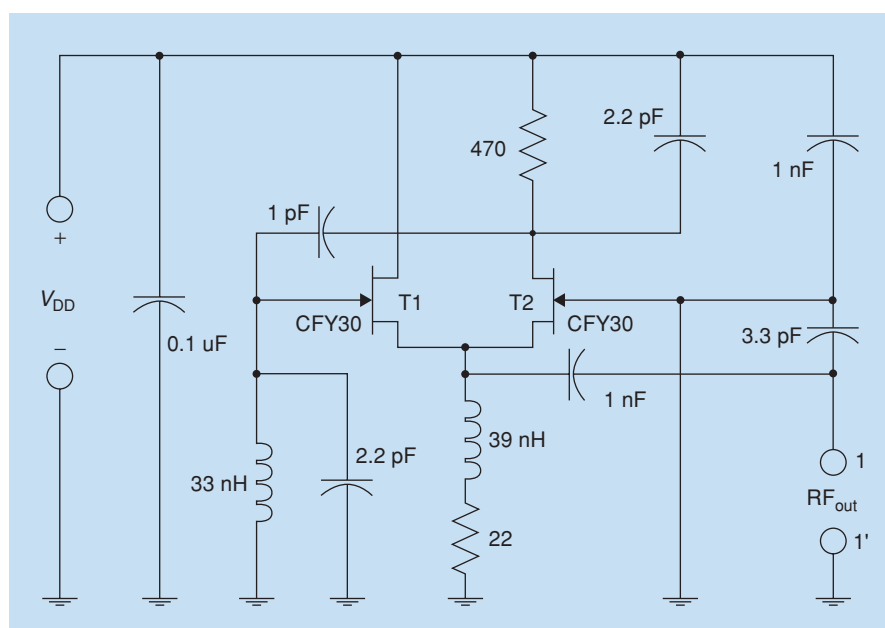


Figure 23. The circuit of the improved oscillator.

oscillator at the target frequency even becomes a little bit smaller, maybe due to the heating up of the transistors at this high amount of supply energy. The measurement results are given in Figure 21 for a frequency range from dc to 2.5 GHz and in Figure 22 for a frequency range from 2.0–10 GHz.

There were no spurious oscillations for any case, which were tested. The only modification to the origin oscillator circuit is one single additional SMD capacitor. This slight modification makes the problematical oscillator circuit that sufficiently works only a low values of the supply voltage to an uncomplicated all-purpose oscillator circuit for all values of the supply voltage up to 5 Vdc. The circuit diagram of the improved oscillator circuit is given in Figure 23.

Conclusions

This article has shed some light upon typical problems of the oscillator design. A number of additional signals can be excited by the oscillator's active kernel due to parasitic effects. These interfere with the projected oscillation frequency or with its harmonics and produce a number of disturbing spurious signals. By the help of a suitable CAD program, such as C/NL2, it is possible to avoid this problem. The CAD program can analyze the reason for these additional oscillations and comfortably give advice how to take measures to inhibit the oscillator's circuit capability to produce these unwanted additional parasitic oscillations. This article examined the problem of exciting spurious emission in an oscillator circuit and proves, that an oscillator can be easily CAD designed and assembled, producing the designed frequency signal, only.

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